A 1/3.4-inch 2.1-Mpixel 240-frames/s CMOS Image Sensor

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***Abstract*- This paper proposes a 240 frames/s 2.1 M-pixel CMOS image sensor with column-shared cyclic ADC that consumes low power of 90 μW/column at 1.5 V supply and is applicable to the fine pixel pitch of 2.25 μm. The prototype sensor was fabricated in a 0.13-μm 1P4M CMOS technology. The measured DNL and INL are +0.59/-0.83 LSB and +2.8/-3.6 LSB, respectively. The measured maximum pixel rate is 500 Mpixels/s with a low power of 300 mW.**

I. INTRODUCTION

A CMOS image sensor covers a large variety of applications from low-cost mobile device to high-end digital camera because it has advantages of the low power consumption and easy system integration with on-chip circuits. Over the last few years, the demand of high density imaging has drastically increased and the shrinking of pixel size has become a major concern to achieve a high pixel density in an adequate optical format. More recently, the application coupled with high pixel density, high-speed videography such as high-definition camcorder and ultrahigh definition TV (UDTV) camera has been actively investigated. The column-parallel architecture is mainly used in high density image sensors with the pixel rate of 200 Mpixels/s or more.

The column-parallel architecture can be grouped by the type of ADC into a single-slope (SS) ADC [1], a successive approximation (SA) ADC [2],[3], and a cyclic ADC [4]-[5]. SS ADCs have been widely applied in a CMOS imager because they provide relatively high resolution with minimal area and low power consumption for a low-speed imager. Although high-speed CMOS imagers based on an SS ADC have been recently reported in [1], they use very high clock frequency which requires high power consumption. SA ADCs have been utilized for high-speed image sensor with 240 frames/s, 4 Mpixels [2] and UDTV sensor with 60 frames/s, 8.9 Mpixels [3]. Since the SA ADC should include a DAC that is proportional to the bit resolution and then occupies a large silicon area, it is not applicable for consumer products. In general, cyclic ADC has the distinct advantage of requiring low power and small area even maintaining moderate conversion speed because it performs the conversion in a serial manner by making repeated use of a simple circuit. This makes the converter suitable to column-parallel readout for a CMOS image sensor.

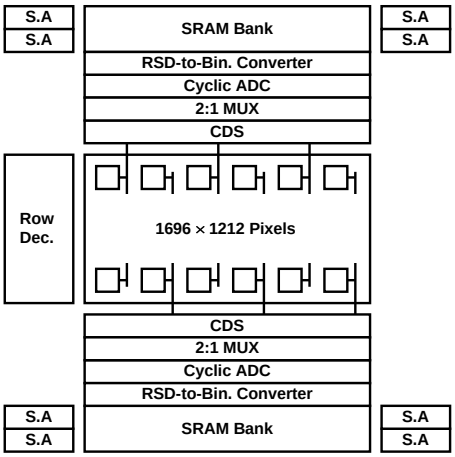


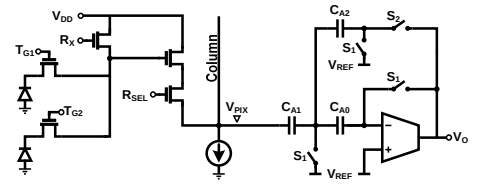
Fig. 1. Overall architecture of the proposed CMOS image sensor.

CMOS image sensors with an improved cyclic ADC, adopting the sharing techniques of the amplifier and capacitor, were reported in [4]-[5]. Although these converters have the excellent resolution of 12 bit or more, they are limited to column readout for VGA image sensor because they still have large column area and high power consumption. Especially, for high density imaging, Low power design is very important because the heat generated by the high power consuming readout circuits increases the temperature of sensor array on the same chip and then the temperature-dependent dark current causes the fixed pattern noise (FPN) and limits the dynamic range of the pixel signal.

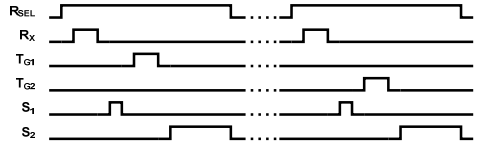
This paper proposes a 240 frames/s, 2.1 Mpixels CMOS image sensor with column-shared cyclic ADC that has a built-in variable gain amplifier without an additional silicon area and operates at 1.5 V supply for low power consumption. Section II presents the architecture of the proposed sensor. Section III provides circuit implementation of the proposed sensor. Section IV shows the experimental results. The conclusion is provided in Section V.

II. ARCHITECTURE

Fig.1 shows the overall architecture of the proposed CMOS image sensor. The sensor is composed of a pixel array, column readout circuits including CDS and ADC, redundant signed digit (RSD)-to-binary converter, SRAM bank for the

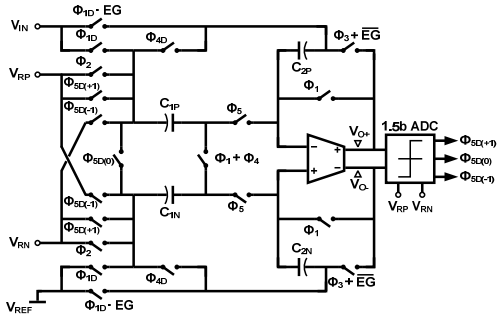


(a)

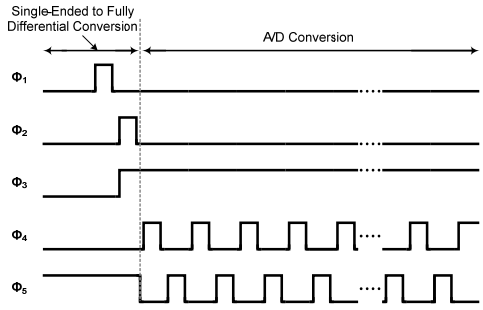


(b)

Fig. 2. Pixel and CDS. (a) Schematic diagram. (b) Timing diagram.



(a)



(b)

Fig. 3. Cyclic ADC with built-in VGA. (a) Schematic diagram. (b) Timing diagram

pipelined row scanning, row decoder, column decoder, and repeater chain. The pixel array consists of 1696×1212 pixels with 2.25-μm pixel pitch implemented by sharing the transistors of two 4T-APS to increase fill factor. In the proposed sensor, to implement readout circuits within the fine pitch, a column shared ADC is multiplexed for two column-CDS circuits. Pixel output is first sampled by the CDS circuit on each column to reduce FPN and then fed to a 10-bit column-shared cyclic ADC. During the A/D conversion, a RSD is sequentially converted to unsigned binary digits by the RSD-to-binary converter. When the conversion is finished, the binary data is shifted into the SRAM. The SRAM is read out through 10-bit, 8 parallel sense amplifiers during the next row time.

III. CIRCUIT IMPLEMENTATION

A. CDS Circuit

To cancel the pixel FPN and reset noise, CDS circuit should be integrated on the column readout. However, column FPN due to the offset variation of the column CDS circuits results in the degradation of the image quality. Fig. 2 shows the schematic and timing diagrams of the proposed CDS used in this CMOS image sensor. The CDS consists of an operational transconductance amplifier (OTA), an offset capacitor (C_{A0}), an input capacitor (C_{A1}), a feedback capacitor (C_{A2}) and 4 switches. When switches controlled by S_1 are turned off before the transfer gate of the pixel turns on, the offset voltage (V_{OS}) of the operational amplifier and the reset level (V_{RST}) of the pixel output are sampled at C_{A0} and C_{A1}, respectively. This operation suppresses the dark signal nonuniformity of the pixel, the reset noise of FD, and the column FPN due to the variation of V_{OS}. When the switch controlled by S_2 is on after the signal level (V_{SIG}) of the pixel is transferred, the difference between V_{RST} and V_{SIG} is transferred on C_{A2}. Regardless of V_{OS}, the resulting signal (V_0) at the output of the CDS circuit is given as follows.

$$V_O = \frac{C_{A1}}{C_{A2}}\Delta_{SIG} + V_{REF} \qquad (1)$$

where Δ_{SIG} is the difference between V_{RST} and V_{SIG}. On the other hand, since the proposed image sensor employs a lower power supply for the ADC than that the power supply of the CDS circuit, the CDS circuit also provides as a level-shifter function using the reference voltage (V_{REF}) to match the signal range of the CDS with that of ADC. Although the CDS can amplify the pixel signal by the ratio of C_{A1}/C_{A2}, it is designed to unity gain in this work because the capacitances of C_{A1} and C_{A2} are chosen to equal value to prevent the saturation of the input signal in the following ADC.

B. Cyclic ADC with Built-in VGA

The schematic and timing diagrams of the proposed cyclic ADC with built-in variable gain amplifier is presented in Fig.3. The proposed ADC consists of an amplifier, 4 capacitors, 2 dynamic latches for 1.5b sub-ADC, and several switches. To improve the power supply noise immunity and to reduce the charge injection, the converter uses the fully-differential configuration. The proposed converter samples the single-ended pixel signal from the CDS and the reference voltage simultaneously through a floating ground to obtain the balanced fully-differential signals and to isolate the coupling noise from a signal ground line shared by all column ADCs. The proposed converter also uses the dynamic latch with a built-in threshold level in which the comparator references (V_P and V_Q) are determined by the width ratio of

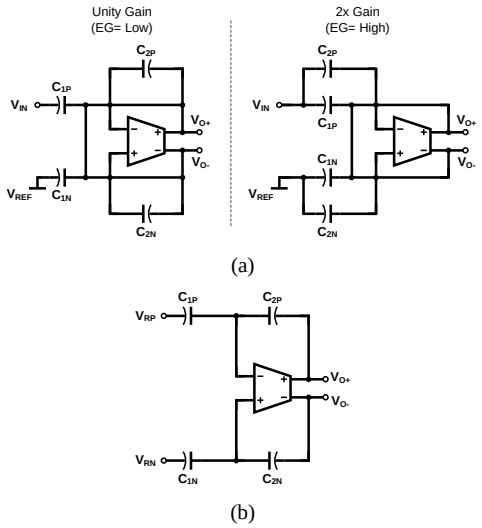


Fig. 4. The circuit configuration for single-ended to fully-differential conversion. (a) Sampling phase. (b) Transfer phase

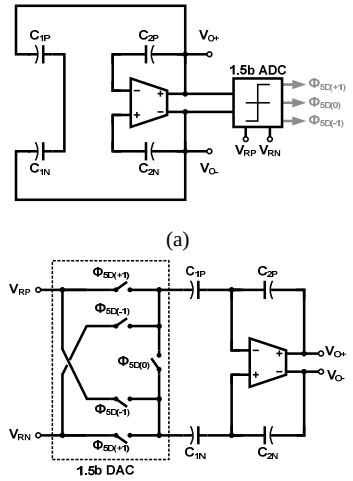


Fig. 5. The circuit configuration for A/D conversion. (a) Sampling phase. (b) Amplification phase.

MOS pairs. This reduces the number of analog reference generators required for comparison.

Fig. 4 shows the circuit configuration for the single-ended to fully-differential conversion. During the sampling phase, the switches controlled by ϕ_1, ϕ_{1D}, and ϕ_5 are turned on as shown in Fig. 4 (a). C_{1P} and C_{1N} sample the CDS output signal and V_{REF}, respectively. On the order hand, the connection of C_{2P} and C_{2N} is provided by the gain mode control (EG). When EG is low, C_{2P} and C_{2N} are discharged. When EG is high, C_{2P} and C_{2N} also sample the CDS output signal and V_{REF}, respectively. During the transfer phase, the switches controlled by ϕ_2, ϕ_3, and ϕ_5 are turned on as illustrated in Fig. 4(b). C_{1P} and C_{1N} are connected to V_{RP} and V_{RN}, respectively.

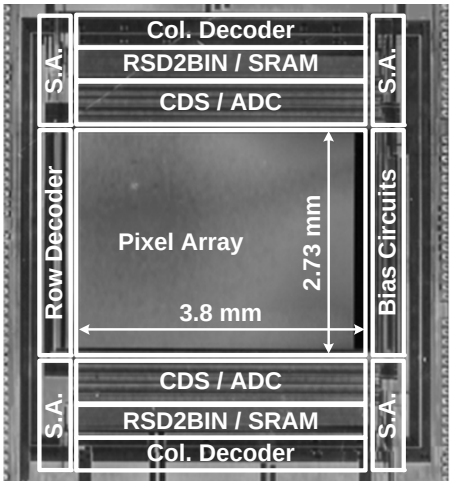


Fig. 6. Chip microphotograph.

C_{2P} and C_{2N} are flip-arounded to the amplifier output. Since the charges on C_{1P} and C_{1N} are transferred into C_{2P} and C_{2N} by the charge conservation, the differential output (V_O) in the case of low EG is expressed as follows.

$$V_O = V_{O+} - V_{O-} = \Delta_{SIG} - V_R \tag{2}$$

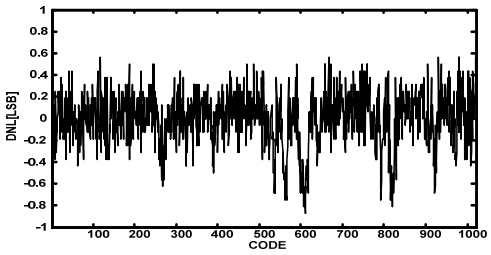
where all capacitances are assumed to be equal and V_R is the difference between V_{RP} and V_{RN}. In the same manner, the differential output in the case of high EG is given as follows.

$$V_O = 2\Delta_{SIG} - V_R \tag{3}$$

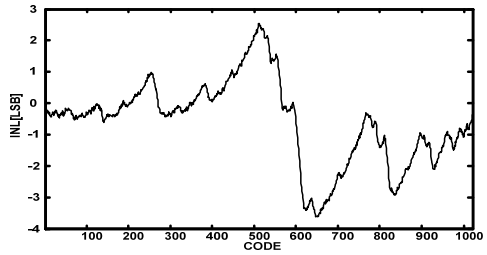
Comparing (5)and (6), the single-ended to fully-differential conversion functions as a VGA that has the gain of one or two according to the gain mode control. The circuit configuration for the A/D conversion is shown in Fig.5. The RSD cyclic algorithm adopted in the converter mitigates the accuracy requirement on comparator and eliminates the non-linear effect of the converter caused by the amplifier offset. This converter has the conversion cycle of 9 times for 10-bit resolution. The proposed ADC provides the built-in VGA without additional silicon area and clock phases and enables the dynamic range enhancement by the maximum gain of the VGA. The power consumption of the proposed cyclic ADC is only 90 μW per column with 1.5V supply voltage. The measured conversion rate is 2 Msamples/s.

III. MEASUREMENT RESULTS

The prototype sensor was fabricated in a 0.13-μm single-poly four-metal CMOS process. The chip microphotograph is shown in Fig. 6. The image array has 1696 ×1212 pixels with 2.25-μm pitch. The length of the implemented CDS/ADC is only 600 μm. ADCs and memories are split between the top and the bottom for symmetry, performance, and optimized routing.



(a)



(b)

Fig. 7. Measured DNL and INL . (a) DNL, (b) INL

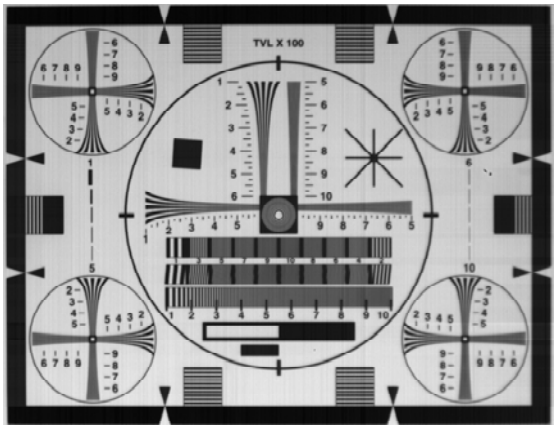


Fig. 8. Sample image.

Fig. 7 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the proposed ADC. The measured DNL and INL are +0.59/-0.83 LSB and +2.8/-3.6 LSB. The conversion time of the proposed ADC is 0.5 μs. Fig. 8 shows the sample image captured from the prototype image sensor at 240 frames/s. The measured column FPN is under 0.1% at dark condition. The maximum pixel rate is 500 Mpixels/s. The power consumption of the prototype sensor is 300 mW.

$$\text{FOM} = \frac{\text{Power}}{\text{pixel rate}} \ [\text{mW/(Mpixels/sec)}] \qquad (4)$$

The FOM of the proposed image sensor with column-shared cyclic ADC is 0.61 mW/(Mpixels/sec). The best FOMs of the image sensors with column SA ADC [1] and SS ADC [2] are 0.72 and 0.94 mW/(Mpixels/sec), respectively. This shows that the proposed sensor is more power efficient than the other sensors with different types of column readouts.

IV. CONCLUSION

This paper proposed a 240 frames/s 2.1 M-pixels CMOS image sensor with column-shared cyclic ADC which provides high speed conversion rate with the low power consumption of 90μW and can be integrated with the fine pixel pitch of 2.25-μm. The proposed sensor is applicable to the high-speed, high density imaging and machine vision.

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